App. Serial No 10/539,224 Docket No.: BE020043US1

In the Claims:

Please amend claim 1 as indicated below. This listing of claims replaces all prior versions.

1. (Currently amended) A method of manufacturing a semiconductor device with a semiconductor body of a semiconductor material, the semiconductor device including a field effect transistor having a source region and a drain region at a surface of the semiconductor body, and having a gate region between the source region and the drain region, the gate region including a semiconductor region of a further semiconductor material that is separated from the surface of the semiconductor body by a gate dielectric, the method comprising:

forming the gate dielectric on the surface of the semiconductor body; forming the semiconductor region on the gate dielectric;

depositing a sacrificial region on top of the semiconductor region;

after depositing the sacrificial region, forming spacers adjacent to the gate region for forming the source and drain regions;

forming the source and drain regions on the surface of the semiconductor body; after forming the source and drain regions, selectively etching the sacrificial region with respect to the semiconductor region;

depositing a metal layer on the source region, the drain region, and the gate region;

forming a compound, that includes at least a portion of the source and drain regions, of the metal layer and the semiconductor material; and

forming a compound, that includes at least a substantial portion of the <u>further</u> <u>semiconductor material</u> <u>gate region</u>, of the metal layer and the further semiconductor material.

2. (*Previously presented*) A method as claimed in claim 1, characterized in that the spacers are formed by depositing a layer of a dielectric material on top of the semiconductor body on which the gate region comprising the semiconductor region and

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the sacrificial region is present and by subsequently removing the deposited layer on top of and on both sides of the gate region by etching.

- 3. (*Previously presented*) A method as claimed in claim 1, characterized in that the further semiconductor region is completely consumed during the formation of the compound of the metal layer and the further semiconductor material.
- 4. (*Previously presented*) A method as claimed in claim 1, characterized in that the formation of the compounds between the metal and the semiconductor material and the metal and the further semiconductor material is carried out in two separate heating steps,

the first heating step resulting in an intermediate compound with a low content of the semiconductor material or of the further semiconductor material and in

the second heating step the intermediate compound being converted to the compound having a higher content of the semiconductor material or of the further semiconductor material.

- 5. (*Previously presented*) A method as claimed in claim 4, characterized in that between the two heating steps, a part of the metal layer which has not reacted to form the intermediate compound is removed by etching.
- 6. (*Previously presented*) A method as claimed in claim 4, characterized in that between the two heating steps, a layer of the further semiconductor material is deposited on the surface of the semiconductor body.
- 7. (*Previously presented*) A method as claimed in claim 6, characterized in that after the second heating step, a part of the layer of the further semiconductor material which has not reacted to form the compound is removed by etching.
- 8. (*Previously presented*) A method as claimed in claim 1, characterized in that after the formation of the compounds of the metal and the semiconductor material and of the metal and the further semiconductor material, the spacers are removed.

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9. (*Previously presented*) A method as claimed in claim 4, characterized in that for the semiconductor material as well as for the further semiconductor material silicon is chosen, and for the intermediate compound and for the compound of the metal and the semiconductor material and the further semiconductor material a metal silicide is chosen.

10. (*Previously presented*) A semiconductor device comprising a field effect transistor obtained by a method as claimed in anyone of the preceding claims.